In the Specification:

Please amend Paragraph [0032] as follows:

[0032] Referring to FIG. 5A hereafter, it is a block diagram illustrating a driving stage of LCD driving circuit according to one preferred embodiment of the present invention. The driving stage includes a dynamic register 506, which couples the clock input 503 to the level shifter 509, for determining if turning on the path between the clock input 503 and the level shifter 509 upon a control signal ~~module~~ 515. Referring to FIG. 5B herein, it is a diagram illustrating level shifting of a driving circuit for LCD driving circuit of the present invention. The operation of the level shifting means is similar to that of FIG. 4. According to formula $P=fcV^2$, dynamic power dissipation is in proportion to square V, which means when the voltage level is half of the original, the power is ideally quarter of the original consumption, thus the driving stage consumes substantially less power on the clock propagation line.